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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,365	03/22/2004	Toshihiro Tanaka	XA-10057	9482

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EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	**PAPER NUMBER**
2824	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/805,365	TANAKA ET AL.
	Examiner	Art Unit
	VanThu Nguyen	2824

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 9* is/are rejected.

7)☒ Claim(s) *2-8,10-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, both current supply control transistor and current absorption control transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claims 1, 2, 9, 10, 17 claim for a current supply control transistor **and** a current absorption control transistor, but FIGS. 2, 6-7, 10 show only transistor 12 which operates in saturated current area of the I-V characteristics.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

See Abstract, line 1.

4. The Specification is objected to because claims 1, 2, 9, 10, 17 claim for a current supply control transistor **and** a current absorption control transistor, but Specification describes, page 13 lines 4-6, the current supply control transistor is the current absorption control transistor.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Onakado et al. (U.S. Patent No. 5,818,761, referring hereafter as Onakado) or Hoang (U.S. Patent No. 5,852,578, referring hereafter as Hoang)

Regarding claim 1, Onakado discloses, in FIG. 36, a non-volatile semiconductor memory device comprising:

a current supply control transistor (e.g. NSG0) disposed between a voltage source (e.g. Vc) and a non-volatile memory cell (e.g. MC0) and connected serially to said voltage source and said non-volatile memory cell; and

an inherent current absorption control transistor (inherent switches connected to source line SL, see FIG. 19 for example, which provides reference voltage during data writing, see FIG. 18D for example) disposed between said non-volatile memory cell and an inherent reference potential (e.g. 1.5V, see FIG. 18D) and connected serially to said non-volatile memory cell and said reference potential;

wherein said current supply control transistor or said current absorption control transistor is operated in a current saturation area denoted by current-voltage characteristics (see FIGS. 4-5 how transistor NSG operates in current saturation area), thereby controlling a current that flows in said non-volatile memory cell at data writing.

(See column 14 line 51 to column 15 line 9)

Regarding claim 1, Hoang discloses, in FIG. 9, a non-volatile semiconductor memory device comprising:

a current supply control transistor (e.g. T3) disposed between a voltage source (e.g. Vcc) and a non-volatile memory cell (e.g. selected memory cell FG3) and connected serially to said voltage source and said non-volatile memory cell; and

a current absorption control transistor (e.g. T5) disposed between said non-volatile memory cell and a reference potential (e.g. ground 95) and connected serially to said non-volatile memory cell and said reference potential;

wherein said current supply control transistor or said current absorption control transistor is operated in a current saturation area denoted by current-voltage characteristics (a constant current sink Iprog through T5 from BL, i.e. T% is operated in its current saturation area), thereby controlling a current that flows in said non-volatile memory cell at data writing (see column 4, lines 6-11).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Onakado/Hoang in view of Yamaki et al. (U.S. Patent No. 6,643,193, referring hereafter as Yamaki).

Regarding claim 9, Onakado/Hoang discloses a semiconductor integrated circuit device including a non-volatile storage with same limitations as applied to claim 1 above.

However, Onakado/Hoang does not teach said semiconductor integrated circuit includes a central processing unit.

Yamaki disclose, in FIGS. 31(A) and 32, a semiconductor integrated circuit includes a central processing unit CPU 71, which gives instructions to non-volatile memory 13NV to execute operations via control signals CEb, EOb, WEb, SC, RESb, CDEb, etc.

Since Onakado/Hoang and Yamaki are all from the same field of endeavor, the purpose disclosed by Yamaki would have been recognized in the pertinent art of Onakado/Hoang.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include a central processing unit in a semiconductor integrated memory device because it is a essential component for controlling memory operations.

Allowable Subject Matter

9. Claims 2-8 and 10-20 are allowed.

The following is a statement of reasons for the indication of allowance:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Onakado, Hoang, Yamaki and Tailliet et al., taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

As in claims 2 and 10: wherein both of said current supply control transistor and said current absorption control transistor are operated in a current saturation area denoted by current-voltage characteristics, thereby controlling a current that flows in said non-volatile memory cell at data writing.

As in claim 17: wherein said current supply control transistor or said current absorption control transistor is operated in a current saturation area denoted by current-voltage characteristics, thereby controlling a current that flows in said non-volatile memory cell at data writing, and selectively applying either a third voltage lower than said second voltage or a fourth voltage lower than said third voltage to the control gate of said control transistor as said first voltage selectively.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 16, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824